Hall Ticket Number:

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VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (E.C.E.) III Year II-Semester Advanced Supplementary Examinations, June/July-2017

Computer Organization and Architecture

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Write a comparative note on 3rd and 4th generation computers.
2. Define computer organization.
3. What are the operations to be performed by a computer during the execution of interrupt cycle?
4. List the phases of instruction cycle.
5. Distinguish between a direct and indirect addressing modes.
6. Represent how CPU evaluates the given arithmetic operation 45*67*+ using stack operations.
7. Explain the Handshaking method of asynchronous data transfer.
8. Define the following terms in perspective of DMA type of data transfer
   a) Burst mode b) Cycle stealing.
9. Define the following terms a) locality of reference b) address space
10. Define the performance of cache memory in terms of hit ratio with suitable example.

Part-B (5 × 10 = 50 Marks)

11. a) Draw a flow chart to explain how addition and subtraction of two fixed point numbers can be done. Give an example to explain it. [5]
    b) Perform signed multiplication of -3 and 7 using booth multiplication algorithm. Represent the numbers in 5 bits including sign bit. Represent the step by step multiplication process. [5]
12. a) Explain the working of control unit of basic computer system with a suitable diagram. [6]
    b) What do you understand by interrupt? What is the difference between a subroutine and interrupt-service routine? [4]
13. a) Define parallel processing and what are the different types of parallel processing? How parallelism can be achieved in uni-processor system? [5]
    b) Compare CISC and RISC. [5]
14. a) Define I/O interface. What are the functions of an I/O interface? [4]
    b) Explain in detail with the help of a diagram the working of daisy chaining with multiple priority levels and multiple devices in each level. [6]
15. a) List the 3 types of mapping process in cache memory. Explain the direct mapping technique of mapping Main memory and cache memory address? [5]
    b) Explain a method of translating virtual address of a program into physical address with the help of a diagram? [5]

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16. a) List the capabilities of micro program sequencer. [4]

    b) Explain restoring division algorithm for fixed point numbers with suitable example. [6]

17. Answer any ***two*** of the following:

    a) Write a short note on Vector processing. [5]

    b) Explain priority encoder method in interrupt initiated I/O? [5]

    c) Illustrate the necessity of Memory Management hardware in a computer system. [5]